IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Xiaoju Wu, et al.	Docket No:	TI-31214
Serial No:	10/017,990	Conf. No:	8404
Examiner:	Dana Farahani	Art Unit:	2814
Filed:	12/14/2001		
For:	BIPOLAR JUNCTION TRANSISTOR WITH ELECTRICAL HOLE ISOLATOR		

REPLY BRIEF

Mail Stop Appeal Brief - Patents
Commissioner For Patents
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Ann Trent
Ann Trent

Dear Sir:

The following Reply Brief is respectfully submitted in triplicate and in connection with the above identified application in response to the Examiner's Answer mailed November 4, 2003.

REMARKS

Are claims 1, 2, 4-6, 8, 13, 15, 17, 21-24, 27, 29, and 30 properly rejected under 35 U.S.C. 102(b) as being anticipated by Husher?

Appellants maintain that claims 1, 2, 4-6, 8, 13, 15, 17, 21-24, 27, 29, and 30 are not properly rejected under 35 U.S.C. 102(b) as being anticipated by Husher.

In responding to the appellants assertion that,

> The word well refers to a region that has a specific function and can be formed by a number of different methods including ion implantation, thermal diffusion etc. The word well in the semiconductor arts refers to a region formed in a semiconductor in which an electronic device is formed.

the examiner states that "every region in a semiconductor device (or substrate) has a specific function, otherwise it would not be in the device." While this statement is factually true, it is completely irrelevant in determining whether the term "well" is a term of art that refers to a specific region. In Appendix I, which is attached to the reply brief, the appellant has reproduced selected pages from a classic text on very large scale integration (VLSI) technology. As described in the preface of appendix I on page xi, the book is intended as a text book for senior undergraduate or first year graduate students in applied physics, etc. The second edition of VLSI Technology was in wide use and circulation before the filing date of the disclosure on appeal. In Figure 13(c) on page 484 of Appendix I, a cross-section diagram of a twin-tub (or twin well) CMOS process is shown. On page 485 of Appendix I, a description of the fabrication process sequence for the twin tub (well) process shown in Figure 14 is described. At the beginning of the second paragraph on page 485 the text clearly states that the words tub and well are used interchangeably to describe the tub (well) regions shown in Figure 14. As shown in Figure 14, the PMOS and NMOS transistors are formed in the n-well (tub) and p-well

(tub) regions respectively. The description of the well (tub) region in a semiconductor integrated circuit given in Appendix I, and taught in schools for over fifteen years, is consistent with the definition given by the appellant in the appellants brief and contradicts the examiners assertions.

The examiner further states that, "while an electronic device or devices might be formed in a well region, this is not necessary. The word "well" is a broad term that could be any doped region in a semiconductor substrate. "The examiner then cites US patent 5,828,124 to Villa to support this statement. In the Villa patent the examiner correctly points out that in Figure 3, the Villa patent refers to region 46' as a well region. The examiner also correctly states that the Villa patent refers to region 48 in Figure 2 as a well region. The examiner then argues that, based on the Villa patent, calling region 160 of the Husher reference a 'well" region is in line with what is commonly understood to be a well region in the art. The examiner is incorrect in his conclusion and the appellant will now show that the Villa patent is consistent with the arguments presented in the appellant's brief.

In Appendix II, which is attached to the reply brief, the appellant has reproduced selected pages from a classic text on Silicon Processing for the VLSI Era, Volume II. The text is used as a text book in many colleges and as a reference book throughout the semiconductor industry. The text has been in circulation since the early nineties. The relevant section, starting on page 534 in Appendix II, describes high performance BiCMOS technology. BiCMOS is a technology that incorporates CMOS transistors and bipolar transistors in the same integrated circuit. Figure 7-58 on page 534 of Appendix II shows process flows for CMOS technology, bipolar technologies and the BiCMOS technology. In the CMOS process flow, the NMOS and PMOS transistors that comprise the CMOS circuit are formed in the p-well and n-well regions respectively. Well regions are not traditionally used in bipolar technologies but Figure 7-58 shows that the wells from the CMOS technology are incorporated into the bipolar transistor. This is further illustrated in Figure 7-59(b) where a cross-section of a twin-well BiCMOS structure is shown. The n-well region in which the PMOS transistor is formed is also formed as part

of the bipolar transistor structure. As clearly shown in the Figure, the region retains the name "well" even though it is now a part of the bipolar transistor structure. The n-well regions in the PMOS transistor and the bipolar transistor are formed simultaneously. This is described in pages 538-543 of Appendix II and illustrated in Figures 7-61, 7-63, and 7-65. It is therefore well established that the term "well" refers to a region in a semiconductor that has a specific function. In BiCMOS technologies the term well is used to describe the regions that are formed simultaneously with the CMOS well regions. As such the term "well" does not describe any arbitrary region as described by the examiner. As shown above the term "well" has a clearly defined meaning in the semiconductor arts.

With regard to the use of the term 'well" in the Villa patent, Figure 2 of the Villa patent shows a region 48 that is described in the disclosure as a p-type well region. The examiner then points to region 46' in Figure 3 that is also described in the disclosure as a well region. The examiner describes region 46' as just a doped region in the device, and describes region 48 as yet another p-doped region in the device. This observation is not supported by the Villa patent where in col 3, lines 63-65 it states, "[A]nnular region 46' is formed using the same mask as for well region 48, so the channel width W_B' is unaffected by misalignment of the masks." The use of the term 'well" to describe regions 46' and 48 well is therefore consistent with recognized use of the term. Both regions are formed simultaneously with the same mask during the formation of the well regions in other parts of the integrated circuit. This is further described in the Villa patent in col. 4, lines 36-40, where it states, "[T]ub-like regions 66 and annular region 67 are formed in the same process steps for forming P-wells of the integrated circuit including the present transistor, and thus do not require specific masking or depositing steps." This statement encompasses the integration of CMOS and bipolar transistors described above. The Villa patent therefore does not stand for the idea that the term "well" can be used to describe any random region as outline by the examiner. The use of the term "well" in the Villa patent is consistent with both the use of the term in the appellant's claims and with the recognized use of the term in the semiconductor arts.

In the alternative, if it is found that the Villa patent uses the term "well" in a way that is different from the recognized use of the term in the semiconductor art, this use would be specific to the Villa patent and to the specific region described in the Villa patent. The regions referred to as well regions in the Villa patent are clearly different from the well regions in the instant invention and the sinker region 160 in the Husher reference. Therefore if it is found that, acting as its own lexicographer, the Villa patent uses the term "well" in a unique way, such use describes different regions in the transistor and would not be relevant to the regions at issue in this appeal.

The Husher patent therefore does not contain all the required elements of claim 1 of the instant invention and claim 1 is allowable over the cited art. Independent claim 22 contains the limitation of forming a well in the first layer. As described above, the Husher patent does not describe a well region and therefore does not describing forming a well region. Independent claim 22 is therefore allowable over the cited art. Furthermore dependent claims 2, 4-6, 8, 13, 15, 17, and 21 depend from claim 1 and therefore contain the limitation of a well. Dependent claims 2, 4-6, 8, 13, 15, 17, and 21 are therefore allowable over the cited art. Dependent claims 23-24, 27, 29, and 30 depend from claim 22 and therefore contain the limitation of forming a well. Dependent claims 23-24, 27, 29, and 30 are therefore allowable over the cited art.

Are claims 3, 7, 10, 14, 25, 26, and 28 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, as applied to claim 1, and further in view of Taniguch?

Appellant maintains that claims 3, 7, 10, 14, 25, 26, and 28 are not properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher as applied to claim 1 in further view of Taniguchi.

As described above claim 1 is allowable over the Husher patent. The Taniguchi patent does not describe a well as required by the claims and therefore claims 3, 7, 10, 14, 25, 26, and 28 are allowable over the Husher patent in further view of Taniguchi.

Are claims 9, 11, 12, 16, 18, 19, and 20 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, as applied to claim 8, and further in view of S.M. Sze, Semiconductor Devices, Physics and Technology?

Appellant maintains that claims 9, 11, 12, 16, 18, 19, and 20 are not properly rejected under 35 U.S.C. 103(a) as being unpatentable over Husher, as applied to claim 8, and further in view of S.M. Sze, Semiconductor Devices, Physics and Technology?

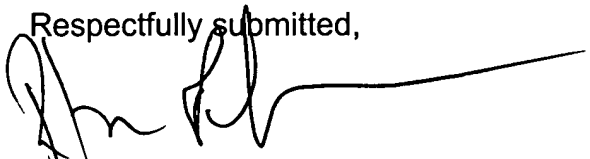
As described above claim 1 is allowable over the cited art. Claim 8 depends on claim 1 and is also allowable over the prior art. Claims 9, 11, 12, 16, 18, 19, and 20 depend on claim 8 and are allowable over the cited art.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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